IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

1. (Previously Presented) A system for identifying pixels inside a graphics primitive of a raster image, the system comprising:

a memory for storing a raster image; and

a graphics engine coupled to the memory and comprising a pipeline structure, the pipeline structure comprising a first plurality of sequential logic circuits coupled in series and a second plurality of parallel logic circuits coupled to the first plurality of sequential logic circuits, each of the sequential logic circuits and each of the parallel logic circuits configured to receive a different polygonal portion of the raster image and to determine whether the received polygonal portion is at least partly inside the graphics primitive.

2. (Cancelled)

3. (Previously Presented) The system of claim 1 wherein the pipeline structure is further configured to divide the polygonal portion into a predetermined number of polygonal subportions if the polygonal portion is at least partly inside the graphics primitive.

4. (Previously Presented) The system of claim 1 wherein the pipeline structure determines whether the polygonal portion of the raster image is at least partly inside the graphics primitive by evaluating edge functions of the graphics primitive on at least one corner vertex of the polygonal portion.

5. (Previously Presented) The system of claim 4 wherein each edge function of the graphics primitive is a vector function comprising both an x-component and a y-component of a vector normal to the edge function.

6. (Previously Presented) The system of claim 4 wherein the edge functions are evaluated on at least one corner vertex of the polygonal portion to determine a corner vertex of the polygonal portion being farthest from a primitive edge associated with the edge function in a direction toward the inside of the graphics primitive.

7. (Previously Presented) The system of claim 1, wherein the sequential logic circuits are followed by the parallel logic circuits.

8. (Previously Presented) The system of claim 1, wherein the parallel logic circuits are coupled together in a pyramid structure.

9. (Previously Presented) The system of claim 3 wherein the predetermined number of polygonal subportions is two and the pipeline structure determines the two polygonal subportions by determining midpoint values of two opposite sides of the polygonal portion of the raster image and using the midpoint values as vertices of the two polygonal subportions.

10. (Previously Presented) The system of claim 1 wherein the pipeline structure further comprises a predetermined number of pixel engines coupled to at least some of the parallel logic circuits and configured to determine attribute values associated with each pixel.

11. (Original) The system of claim 1 wherein the polygonal portion of a raster image has a width ΔX and a height ΔY, each of the width ΔX and the height ΔY having a value of 2^m.

12-21. (Cancelled)

22. (Currently Amended) A method of identifying pixels inside a graphics primitive of a raster image comprising the steps of:

selecting a tile including a pixel;

~~defining a coordinate reference frame for the tile, the coordinate reference frame located at a geometric center of the tile;~~

determining if a portion of the tile is within the graphics primitive;

dividing the tile into two subtiles if a portion of the tile is within the graphics primitive and an other portion of the tile is outside the graphics primitive;

~~relocating the coordinate reference frame to a geometric center of each of the subtiles;~~ and

recursively dividing, over a number of cycles, each subtile larger than a pixel and having a portion within the graphics primitive and an other portion outside the graphics primitive into further subtiles ~~and relocating the coordinate reference frame to a geometric center of each of the further subtiles~~, wherein a maximum number of subtiles processed per cycle is a constant in each cycle of a first plurality of the number of cycles and increases for cycles of a second plurality of the number of cycles.

23. (Cancelled)

24. (Previously Presented) The method of claim 22 wherein the step of determining further comprises evaluating the tile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive.

25. (Previously Presented) The method of claim 22 wherein the step of recursively dividing further comprises determining if the subtile is at least partly within the graphics primitive by evaluating the subtile at a corner vertex which is farthest in a direction toward the inside of the graphics primitive relative to an edge of the graphics primitive.

26-29. (Cancelled)

30. (New) A system for identifying pixels inside a graphics primitive of a raster image, the system comprising:

a memory for storing a raster image; and

a graphics engine coupled to the memory and comprising a pipeline structure including:

a sequential logic block comprising a plurality of identical sequential logic circuits coupled in series and including a first sequential logic circuit and a last sequential logic circuit,

the first sequential logic circuit configured to receive a polygonal portion of the raster image from the memory and to either disregard the polygonal portion if the polygonal portion is outside of the graphics primitive or, if the polygonal portion is at least partly inside the graphics primitive, to subdivide the polygonal portion into equal polygonal subportions and output the polygonal subportions, and

the last sequential logic circuit configured to receive polygonal subportions, disregard any polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining polygonal subportion into further equal polygonal subportions and output those further polygonal subportions; and

a parallel logic block comprising a plurality of identical parallel logic circuits including:

a first parallel logic circuit configured to receive the further polygonal subportions output from the last sequential logic circuit, disregard any further polygonal subportions thereof that are outside of the graphics primitive, and subdivide a remaining further polygonal subportion into still further equal polygonal subportions and output those still further polygonal subportions to two next parallel logic circuits operating in parallel.